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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,989	10/17/2000	Yoshitaka TSUNASHIMA	04329.1952-01000	2408

22852 7590 06/18/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
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WASHINGTON, DC 20005

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,989	TSUNASHIMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27,28 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *27,28 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 132 , requesting a " Request for Continued Examination" (RCE) filed on April 08, 2003 which was entered on April 14, 2003 which papers have been placed of record in the file.

Request for Continued Prosecution Application

The request filed on 04/8/2003 for a Request for Continued Prosecution Application (RCE) under 37 CFR 1. 114 based on parent Application No. 09/688,989 is acceptable and a RCE has been established. An action on the RCE follows.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment(request for reconsideration) filed on 4 /08 /2003, which is identical to the request for reconsideration filed on February 10, 2003 (entered on March 06, 2003) and not found

Therefore claims 27-28 and 30-32 as recited in the amendment of March 11, 2002 are currently pending in the application.

Drawings

The drawings filed on 10/01/00 have been objected to by the draftsperson for the reasons stated in the enclosed PTO-948.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

II. Claims 27, 28, 30- 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 27 the phrase "a side wall of said first gate electrode at one end of a channel direction is connected to a sidewall of said second gate electrode at one end of the channel direction" renders the claim indefinite because the term " the channel " is indefinite since the channel has several meanings and the specification including drawings describe two different gates with two different channels whereas claim 27 as presently recites includes only a single channel between the two gates.

Claims 28,30-33 are rejected at least for depending upon rejected claim 27.

In claim 33, the phrase, " said second gate electrode is formed on the poly silicon layer, and said side wall of said first gate electrode is connected to the side wall of said second gate electrode and a side wall of said side insulator film ." It is not understood what applicants' mean by the phrase, "and said side wall of said first gate electrode is connected to the side wall of said second gate electrode and a side wall of said side insulator film."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27,28 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume et al. (U.S. Patent No. 5,188,976, herein after Kume) and Tada (U.S. Patent NO. 5,497,021 herein after Tada) for reason previously stated (and reproduced below), for response to Applicants' arguments see section below.

With respect to claim 27, to the extent understood, Kume describes substantially all the structure set forth in the claims except the newly added limitation, " a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction '.

However, Tada a patent from the same filed of endeavor, describes in fig. 3(d) and col. 8 lines 1-10 a direct connection between gate electrodes 13 a and b (and also a connection through the interlayer interconnect aluminum layer) (i.e. a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction) to reduce the device size.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Tada's direct connection between gate electrodes 13 a and b (i.e. a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction) in Kume's device to reduce the device size (i.e. miniaturization and reducing the chip area of the semiconductor device Tada col. 8 lines 8-11).

With respect to claim 28, wherein a part of the side wall of the first gate electrode is only connected to a part of the sidewall of the second gate electrode and the part of the side wall of the first gate electrode (Tada fig. 3 d col. 8 lines 1-15, the motivation to combine Kume and Tada given above) and col. and the part of the side wall of the second gate electrode are substantially perpendicular to a surface of the semiconductor substrate . (Kume fig. 18, 35 is perpendicular to 11).

With respect claim 30, to the extent understood, it has not been amended and the previous rejection is maintained.

With respect to claim 31, wherein said first transistor includes a first insulator film and second transistor includes insulator film (Kume fig. 4 # 18-20,col.8 line 15-first and fig.4 # 27, col. 10 line 55-second) and the first insulator film is thinner than the second insulator film, the first transistor in included in a logic circuit and the second transistor is included in a memory cell (Kume figs. 4 and 18).

With respect to claim 32, to the extent understood, wherein top surfaces of the first and second gate electrodes and a connection layer are coplanar . In addition to the obvious design choice rejection stated in the previous office actions and incorporated here by reference (see also Tada fig. 3d and col. 8 lines 5-10).

With respect to claim 33, to the extent understood, wherein the device has a gate insulator formed on the substrate (Kume fig. 4 # 18-20, col. 8 line 15), a poly silicon layer formed on the gate insulator film (Kume figs. 4 and 18, col. 13 lines 40-45) and a side insulator film formed on a side of the gate insulator film and the poly silicon film (Kume fig. 18 # 26, col. 8 line 18-19), the second gate electrode is formed on the and the second gate electrode is formed on the poly silicon layer and the side wall of the first gate electrode is connected to the side wall of the second gate electrode and a side wall of the side insulator film.

Response to Arguments

Applicant's arguments filed 4,08, 2003 have been fully considered but they are not persuasive for the following reasons.

Applicants' contention that the rejection of claim 27 in the previous Office Action fails to show a transistor without an insulation layer between itself and the semi conducting substrate ion which it is formed can function as a transistor is maintained.

Applicants' have not submitted any amendments to amend claim 27 therefore the previous rejection is maintained .

Applicants' previous contention , " figures 10, 13 A-D and 20 B (related text on pages 32, -36,45 and 46) illustrates and describes two transistors which are connected by a sidewall" is also not persuasive for reasons set out below.

However the rejection deals with the lack of an insulation layer between the gate and the semi conducting substrate ion which it is formed and how it can function as a transistor. Therefore its seems that applicants' response to the outstanding 112, first paragraph rejection has not dealt with the issue of the rejection.

Therefore Applicants' arguments are not persuasive and the rejection is maintained .

Claims 28, 30-33 are also rejected at least for depending upon rejected claim 27.

The rejection of claims 27 and dependent claims 28, 30-33 in the previous Office Action based on the recitation, " a side wall of said first gate electrode at one end of a channel direction is connected to a sidewall of said second gate electrode at one end of the channel direction". is also maintained.

Applicants' previous argument that claim 27 is definite because it sets forth the location of the side wall (i.e. One end of the channel) and the phrase when analyzed in light of the disclosure e.g. pages 32-38, 45 and 46 discloses an exemplary location of the sidewall is also not persuasive for reasons set out below.

Applicants' have not submitted any amendments to amend claim 27 therefore the previous rejection is maintained.

Again the alleged location of the sidewall is not the issue, the rejection is based (as previously stated) on the ambiguity of not specifically reciting in the claims which

channel direction the applicants' mean of the possible at least four) by reciting , " a side wall of said first gate electrode at one end of a channel direction is connected to a sidewall of said second gate electrode at one end of the channel direction " thus one cannot determine what direction is included/excluded .

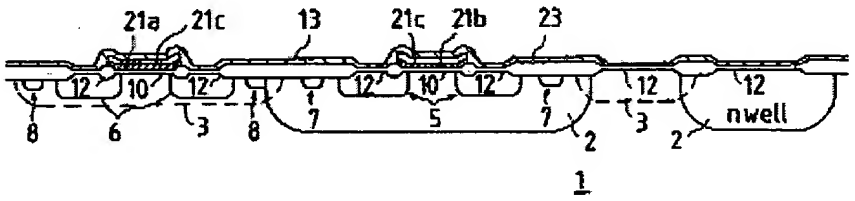
With respect to claim 33 it recites the same claim language as claim 27 (above) and is rejected for the same reasons.

However applicants' arguments that are similar to the arguments under claim 27 are not persuasive for the reasons set out above.

Applicants contend that Tada does not disclose/ suggest that the sidewalls of the gate electrodes are connected.

However Tada in Figure 3D shows element (21) connecting gate electrodes sidewalls 13 a and b. (reproduced below).

FIG. 3(d)



Therefore contrary to applicants' contention all of the presently recited limitations of the claims, including sidewalls of the gate electrodes 13 a and 13 b are connected by element (polysilicon layers) 21 a and 21 b (col. 8 lines 1-11) is taught , (and to the extent understood " a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of said gate electrode at one end of the channel

direction") by Kume and Tada and therefore prima facie obviousness has been established.

Applicants' argument that the applied Tada reference fails to teach" the sidewall of said first gate electrode at one end of the channel is connected to a sidewall of said second gate electrode at one end of the channel direction" because allegedly Tada's fig.3d is not a complete constructed semiconductor device is not persuasive because the structure in fig.3 d is the final structure obtained by steps in figs. 3a- 3d (and is a different embodiment from that described in fig.1), Applicants' argument that fig. 3d does not disclose gate electrode 13 a and b is also not true because the gate structures are clearly shown however not marked, but col. 8 line 1 (reproduced below) clearly identifies 13a and b as gate electrodes. :

> conducting type. Thus, even after the formation of the source-drain diffusion regions **14***a* and **15***a*, the gate electrodes **13***a* and **13***b* are n conducting type polycrystalline silicon layer. Therefore, when a CMOS structure is composed of the low voltage n channel type MOSFET **101** and

Applicants' next contetion that Kume and Tada cannot be combined to produce Applicants' calimed invetion because Tada fails to teach gate elctrodes 13 a and b are connected is not persuasive because Tada as stated above (shows element 21 in fig. 3 D connecting gate lelectrodes sidewalls 13 a and b).

Applicants' next contention that there is no motivation suggestion to combine Kume and Tada is also not persuasive because as previously stated (O/A mailed 06/06/2002 page 6 :

"Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Tada's direct connection between gate electrodes 13 a and b (i.e. a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction) in Kume's device to reduce the device size (i.e. miniaturization and reducing the chip area of the semiconductor device Tada col. 8 lines 8-11)."

It is well known in the semiconductor filed that inventors are constantly trying to reduce the size and this principle is also quantified by the famous Moore's Law.

Therefore clear motivation has/is provided to combine Tada and Kume and a prima facie case of obviousness clearly established.

Applicants' next contention that Tada's gate electrodes 13 a and b are not connected is not persuasive for reasons set out above.

Therefore none of the Applicants' arguments is persuasive .

The dependent claims 28, 30-33 were alleged "to be allowable due to their depndence from allowable claim 1 " . It is noted that claim 1 is cancelled and the claims 28, 30-33 depend upon independet claim 27 not claim1 .

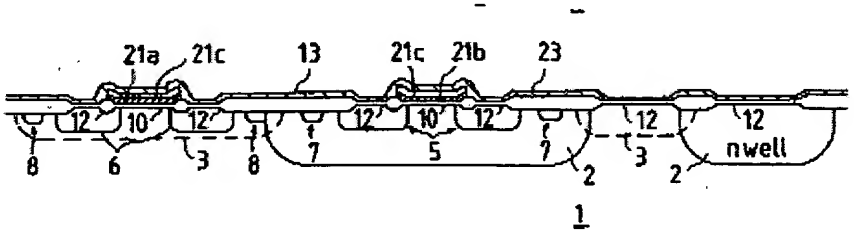
However claim 27 is not allowable for reasons set out above and therefore claims 28, 30-33 are also not allowable.

As stated in the previous Office Action Kume and Tada teach substantially the limitations presently recited . The response to applicants' arguments against the rejection is in the response to the arguments section below.

Applicants contend that Tada does not disclose/ suggest that the sidewalls of the gate electrodes are connected.

However Tada in Figure 3D shows element (21) connecting gate electrodes sidewalls 13 a and b. (reproduced below).

FIG. 3(d)



Therefore contrary to applicants' contention all of the presently recited limitations of the claims, including sidewalls of the gate electrodes 13 a and 13 b are connected by element (polysilicon layers) 21 a and 21 b (col. 8 lines 1-11) is taught , (and to the extent understood " a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of said gate electrode at one end of the channel direction") by Kume and Tada and therefore prima facie obviousness has been established.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner .

June 16, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800